● General Description

The CH50N100N combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

● Features

■ Advance high cell density Trench technology

■Low $R_{DS(ON)}$ to minimize conductive loss

■Low Gate Charge for fast switching ■Low Thermal resistance

●Application

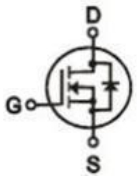
■MB/VGA Vcore

■SMPS 2nd Synchronous Rectifier

■POL application

■BLDC Motor driver

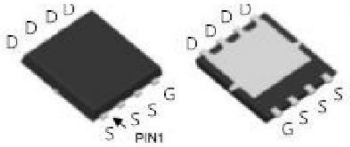
● Product Summary



V_{DS} =100V

$R_{DS(ON)}$ =15mΩ

I_D =55A



DFN5 x 6

●Ordering Information:

Part NO.	CH50N100N
Marking	CH50N100N
Packing Information	REEL TAPE
Basic ordering unit (pcs)	5000

●Absolute Maximum Ratings（T_C =25℃）

Parameter	**Symbol**	Rating	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	20	V
Continuous Drain Current	$I_{D@}$TC=25℃	55	A
	$I_{D@}$TC=75℃	45	A
	$I_{D@}$TC=100℃	35	A
Pulsed Drain Current	I_{DM}	220	A
Total Power Dissipation(TC=25℃)	$P_{D@}$TC=25℃	83	W
Total Power Dissipation(TA=100℃)	$P_{D@}$TC=100℃	50	W
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃
Single Pulse Avalanche Energy@L=0.1mH	E_{AS}	8	mJ
Avalanche Current@L=0.1mH	I_{AS}	150	A

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	1.74		°C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W
Soldering temperature, wavesoldering for 10s	T_{sold}	-	-	125	°C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V,I_D =250uA	100			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	1.4	2.0	2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS} =0V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V ,V_{DS} =0V			±100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		12	15	mΩ
		VGS=4.5V, ID=20A		16	26	mΩ
Forward Transconductance	g_{FS}	V_{DS} =15V, I_D=10A		18		s
Source-drain voltage	V_{SD}	Is=8A			2.90	V

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, F = 1 MHz	-	1441	-	pF
Output capacitance	C_{oss}		-	391	-	
Reverse transfer capacitance	C_{rss}		-	15	-	

●Gate Charge characteristics(T_a = 25°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q_g	V_{DS} =50V	-	20	-	nC
Gate - Source charge	Q_{gs}	I_D = 20A	-	5	-	
Gate - Drain charge	Q_{gd}	V_{GS} = 10V	-	4	-	

Note: ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

Electrical Characteristics Diagrams

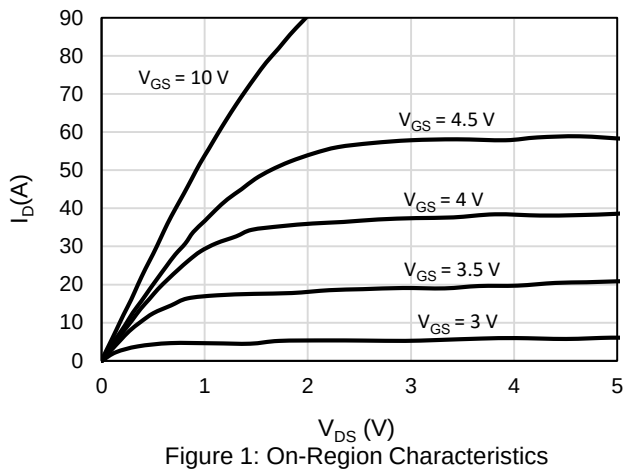


Figure 1: On-Region Characteristics

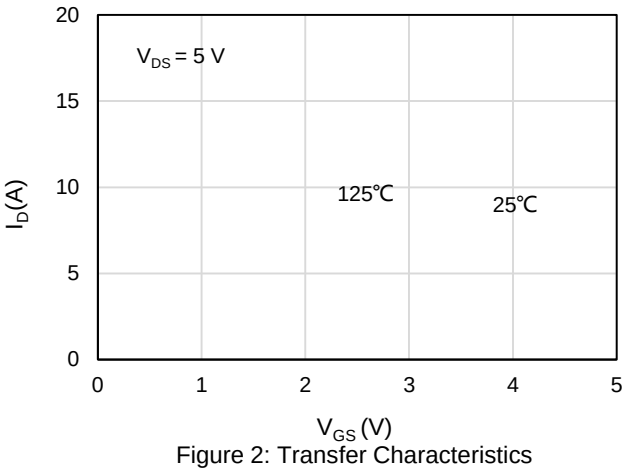


Figure 2: Transfer Characteristics

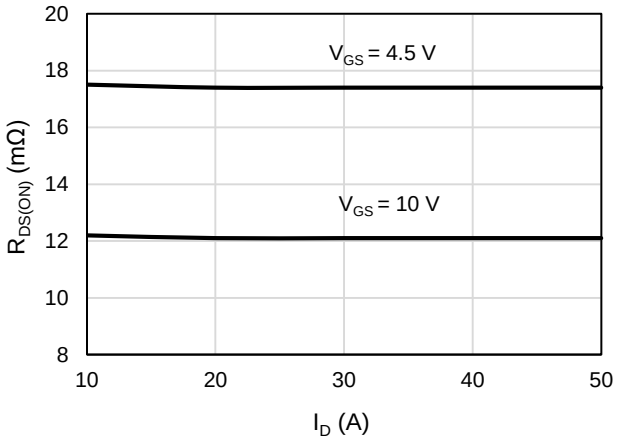


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

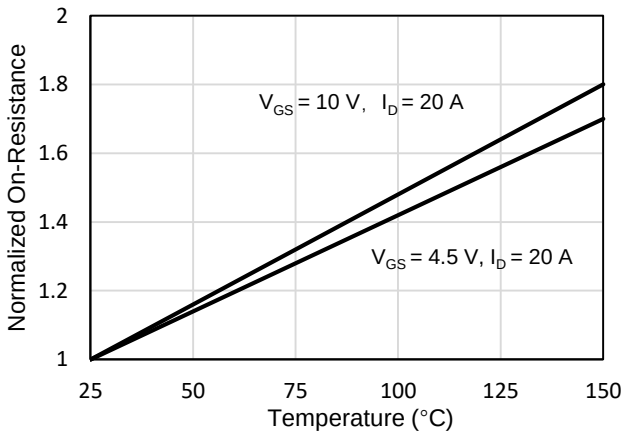


Figure 4: On-Resistance vs. Junction Temperature

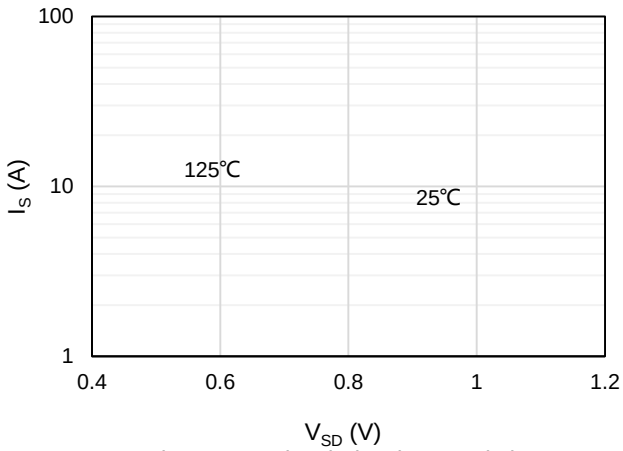


Figure 5: Body-Diode Characteristics

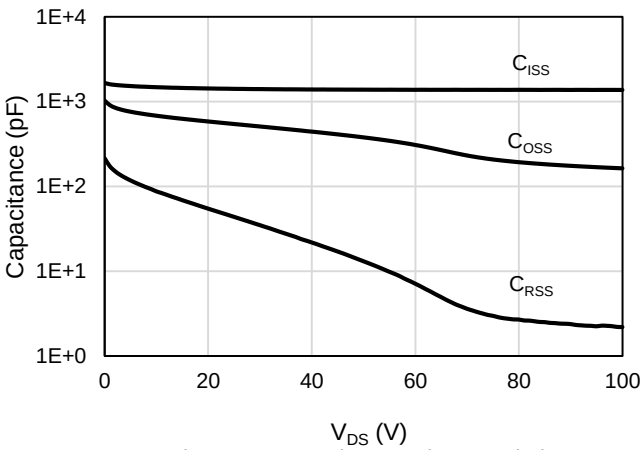


Figure 6: Capacitance Characteristics

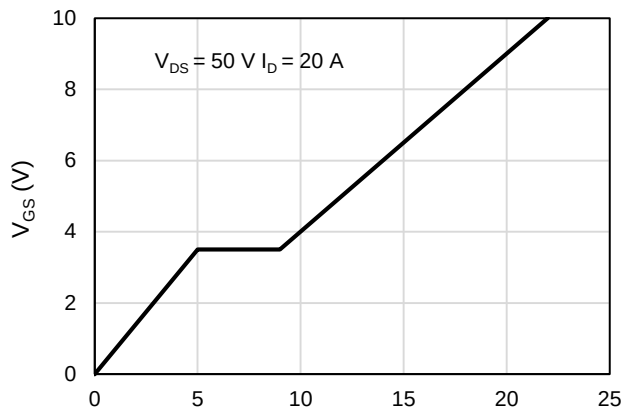


Figure 7: Gate-Charge Characteristics

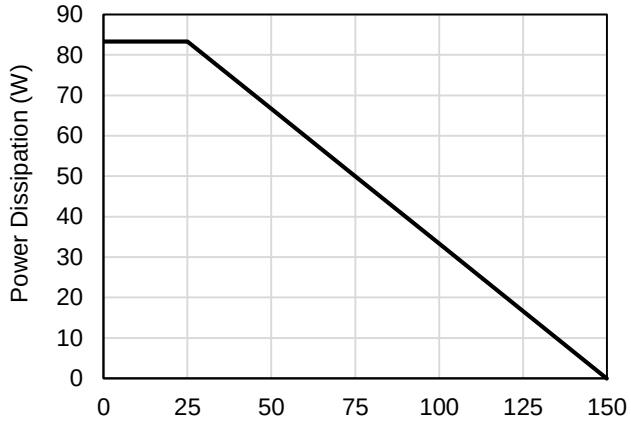


Figure 8: Power De-rating

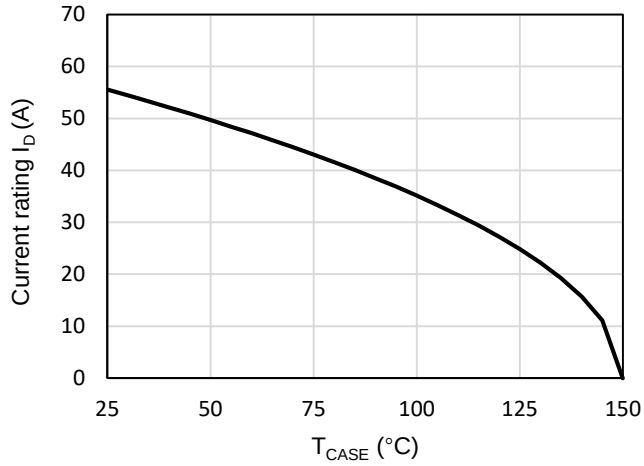


Figure 9: Current De-rating

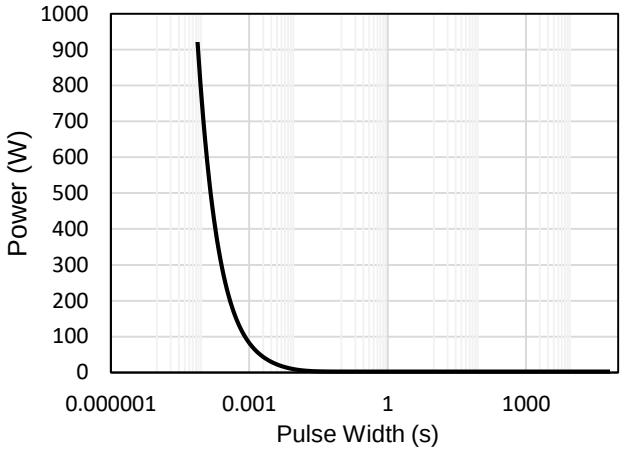


Figure 10: Single Pulse Power Rating Junction-to-Case

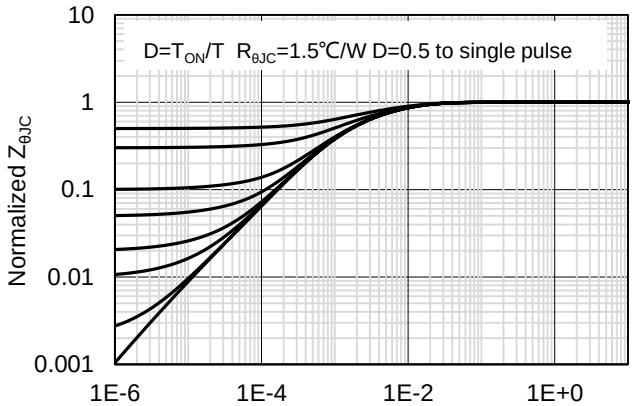


Figure 11: Normalized Maximum Transient Thermal Impedance

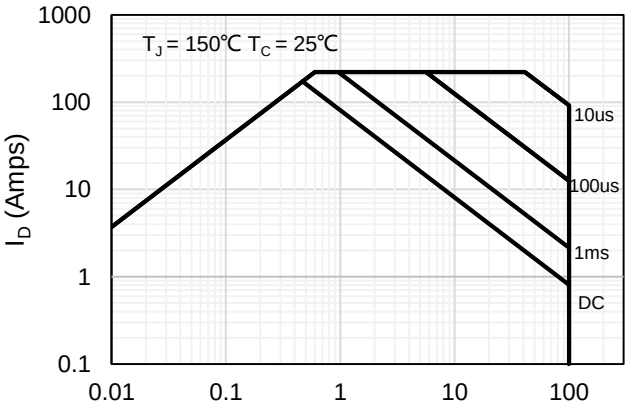
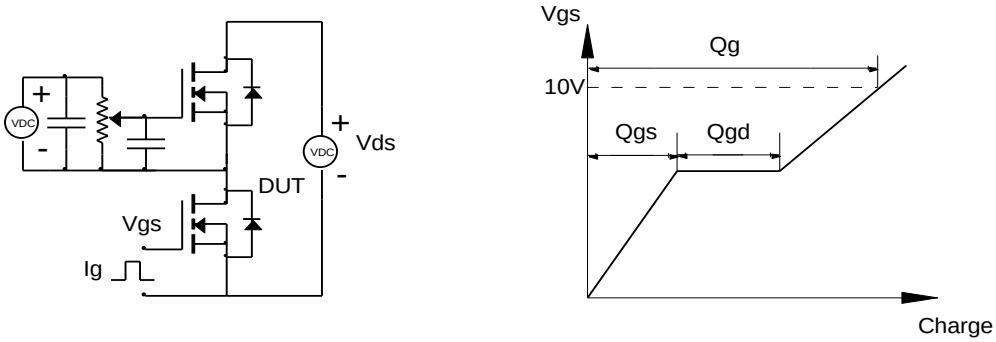


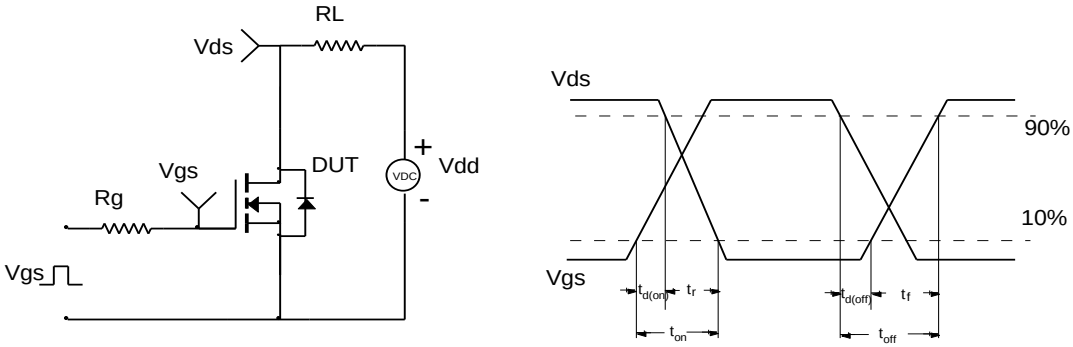
Figure 12: Maximum Forward Biased Safe Operating Area

Test Circuit and Waveform

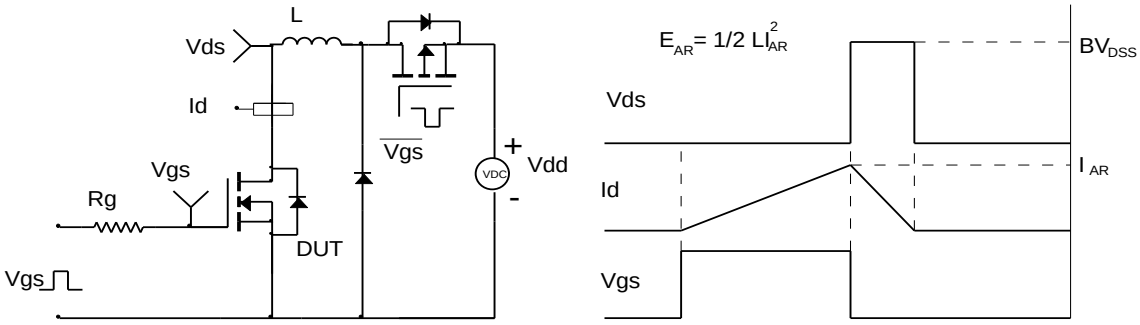
Gate Charge Test Circuit & Waveform



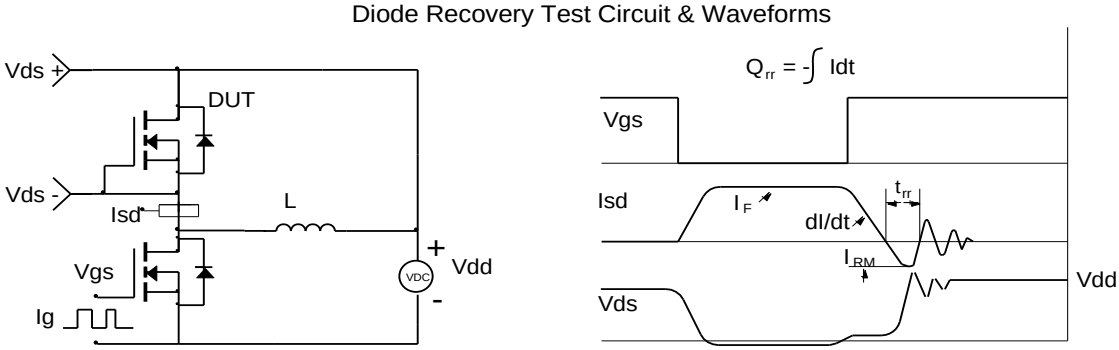
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

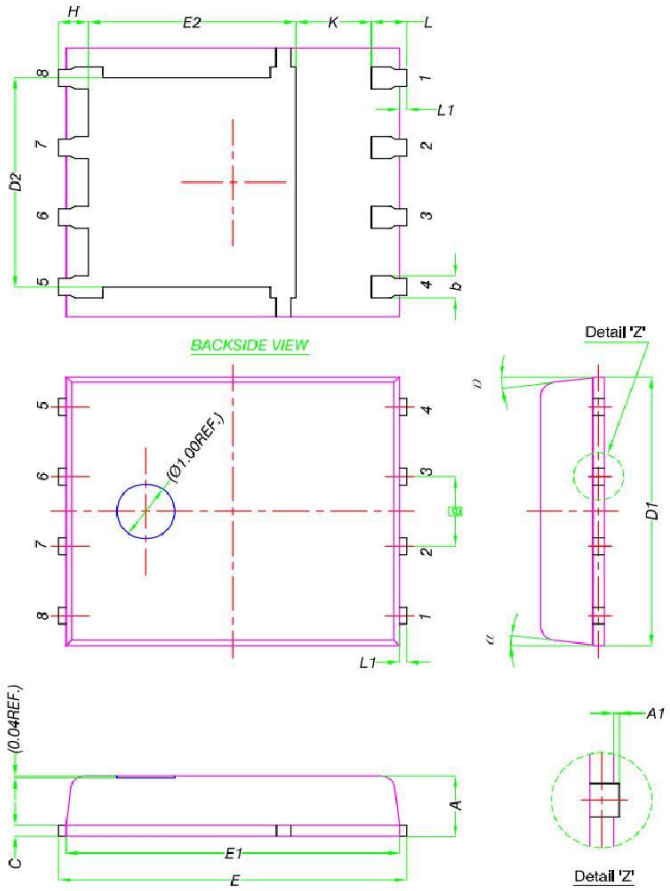


Diode Recovery Test Circuit & Waveforms



●Dimensions（DFN5×6）

Unit：mm



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°