• General Description

The CH30N100N combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

• Features

■ Advance high cell density Trench technology

■Low $R_{DS(ON)}$ to minimize conductive loss

■Low Gate Charge for fast switching ■Low Thermal resistance

•Application

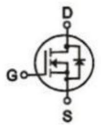
■MB/VGA Vcore

■SMPS 2nd Synchronous Rectifier

■POL application

■BLDC Motor driver

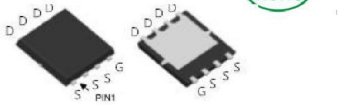
• Product Summary



V_{DS} =100V

$R_{DS(ON)}$ <24 mΩ

I_D =30A



DFN5 x 6

•Ordering Information:

Part NO.	CH30N100N
Marking	CH30N100N
Packing Information	REEL TAPE
Basic ordering unit (pcs)	5000

•Absolute Maximum Ratings (T_C =25℃)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_{D@}$TC=25℃	30	A
	$I_{D@}$TC=75℃	25	A
	$I_{D@}$TC=100℃	20	A
Pulsed Drain Current	I_{DM}	120	A
Total Power Dissipation(TC=25℃)	P_D@TC=25℃	45	W
Total Power Dissipation(TA=100℃)	P_D@TC=100℃	30	W
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃
Single Pulse Avalanche Energy@L=0.1mH	E_{AS}	30	mJ
Avalanche Current@L=0.1mH	I_{AS}	30	A

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	3.0		°C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	68.5	°C/W
Soldering temperature, wavesoldering for 10s	T_{sold}	-	-	125	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V,I_D =250uA	100			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	1.0	1.8	2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS} =0V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V ,V_{DS} =0V			±100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A		20	26	mΩ
		VGS=4.5V, ID=10A		25	31	mΩ
Forward Transconductance	g_{FS}	V_{DS} =15V, I_D=10A		18		s
Source-drain voltage	V_{SD}	Is=8A			1.20	V

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C_{iss}	f = 1MHz V_{DS} =25V	-	660	-	pF
Output capacitance	C_{oss}		-	375	-	
Reverse transfer capacitance	C_{rss}		-	21	-	

•Gate Charge characteristics(T_a = 25℃)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q_g	V_{DS} =50V	-	25	-	nC
Gate - Source charge	Q_{gs}	I_D = 10A	-	6.0	-	
Gate - Drain charge	Q_{gd}	V_{GS} = 10V	-	5.0	-	

Note: ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

Typical Performance Characteristics

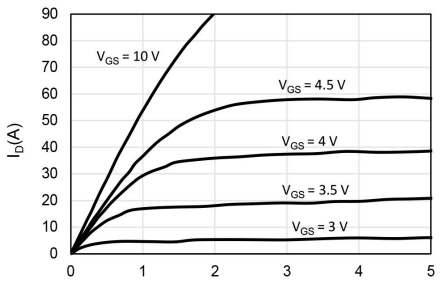


Figure 1: On-Region Characteristics

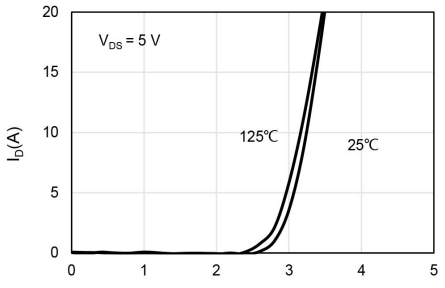


Figure 2: Transfer Characteristics

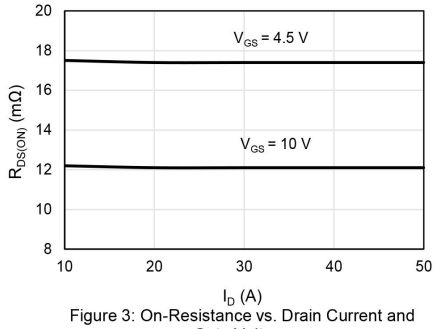


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

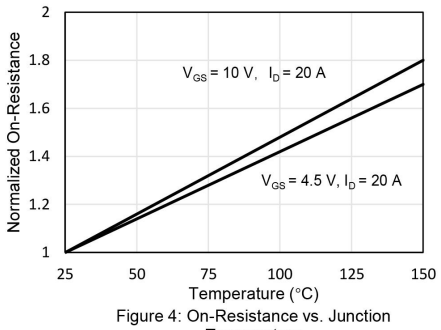


Figure 4: On-Resistance vs. Junction Temperature

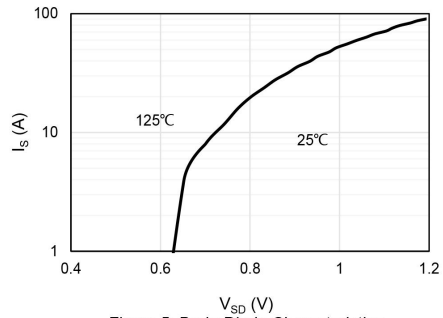


Figure 5: Body-Diode Characteristics

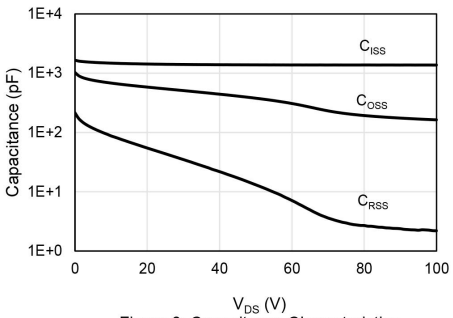


Figure 6: Capacitance Characteristics

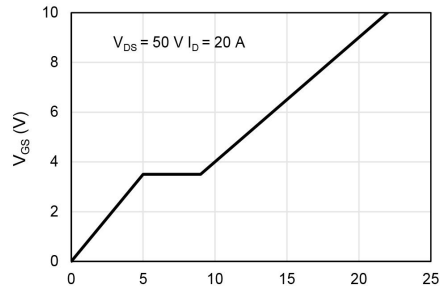


Figure 7: Gate-Charge Characteristics

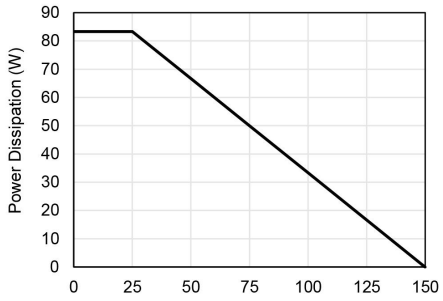


Figure 8: Power De-rating

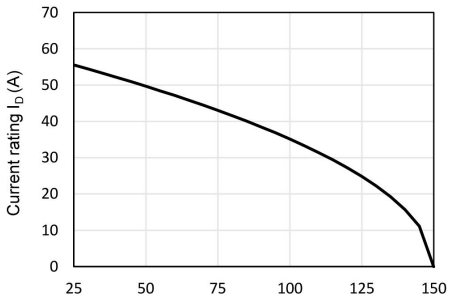


Figure 9: Current De-rating

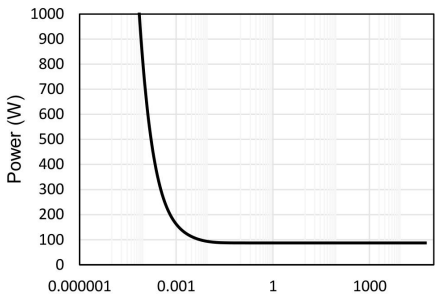


Figure 10: Single Pulse Power Rating Junction-to-Case

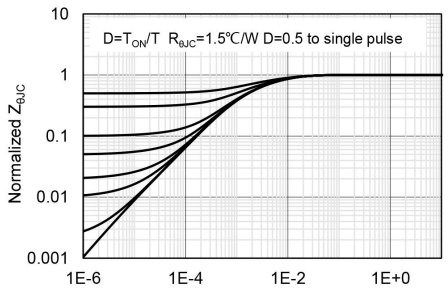


Figure 11: Normalized Maximum Transient Thermal Impedance

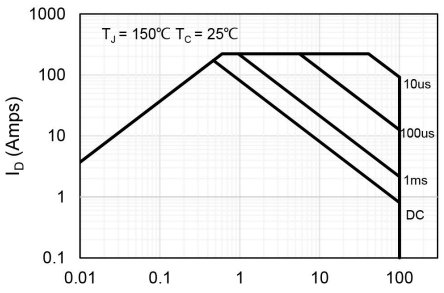


Figure 12: Maximum Forward Biased Safe Operating Area

Test Circuit and Waveform

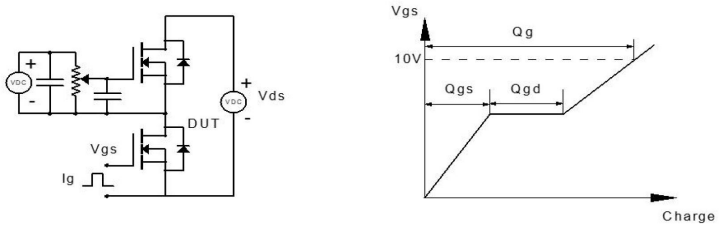


Figure 1: Gate Charge Test Circuit & Waveform

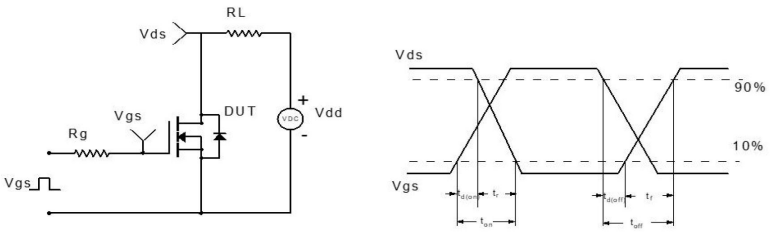


Figure 2: Resistive Switching Test Circuit & Waveform

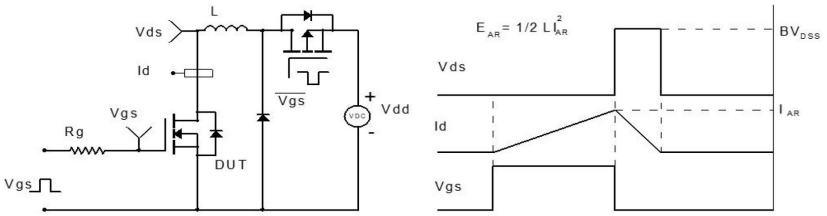


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

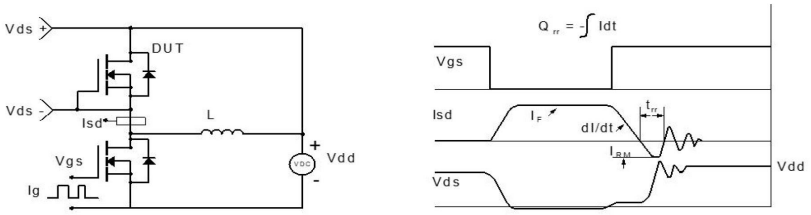
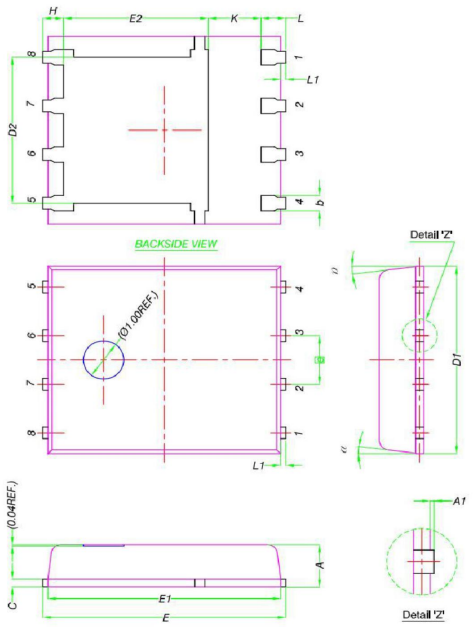


Figure 4: Diode Recovery Test Circuit & Waveform

•Dimensions（DFN5×6）

Unit：mm



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°