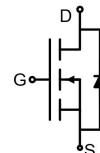


### Description

The CH2N100Q uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

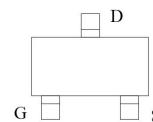
- $V_{DS} = 100V, I_D = 3.0A$
- $R_{DS(ON)} < 286m\Omega$  @  $V_{GS}=10V$
- High density cell design for ultra low Rdson



Schematic diagram

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



SOT-23

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous $T_c=25^\circ C$	$I_D$	3.0	A
Drain Current-Pulsed <sup>(Note 1)</sup> $T_c=25^\circ C$	$I_{DM}$	12	A
Maximum Power Dissipation $T_A=25^\circ C$	$P_D$	2.3	W
Maximum Operating Temperature	$T_J$	150	$^\circ C$
Storage Temperature Range	$T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	54	$^\circ C/W$
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### Electrical Characteristics ( $T_J=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100		-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$	-	-	1	$\mu A$



**CH2N100Q**  
**100V N-Channel Power MOSFET**

Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250µA	1.0	1.5	2.2	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2.0A	-	220	286	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =1.0A	-	250	325	
<b>Dynamic Characteristics</b> (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	321	-	PF
Output Capacitance	C <sub>oss</sub>		-	21	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	15	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V, R <sub>G</sub> =3.0Ω	-	14	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	54	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	18	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	11	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =2A, V <sub>GS</sub> =10V	-	5.3	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.3	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	1.7	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =3.0A	-	-	1.2	V

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

### Typical Performance Characteristics

Figure 1: Output Characteristics

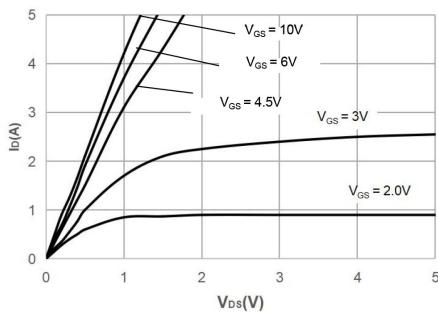


Figure 2: Typical Transfer Characteristics

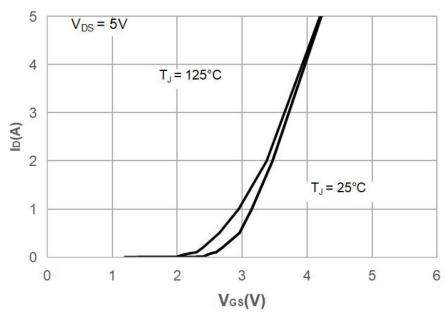


Figure 3: On-resistance vs. Drain Current

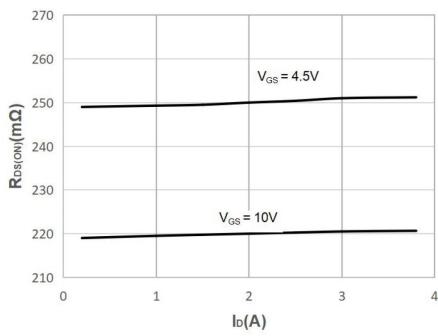


Figure 4: Body Diode Characteristics

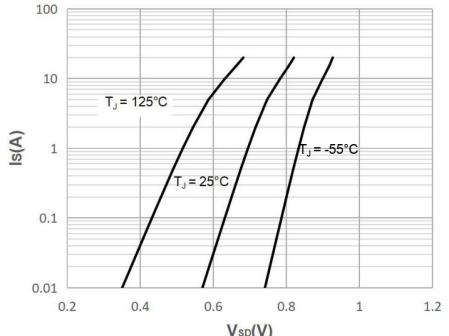


Figure 5: Gate Charge Characteristics

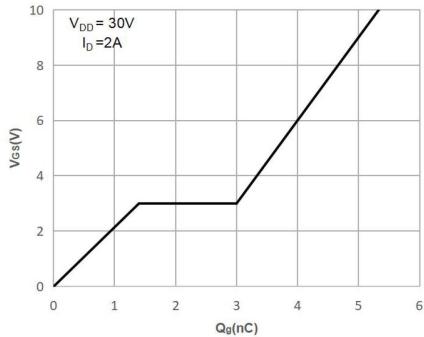
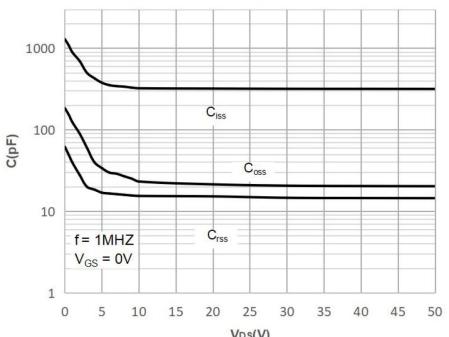


Figure 6: Capacitance Characteristics



## Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

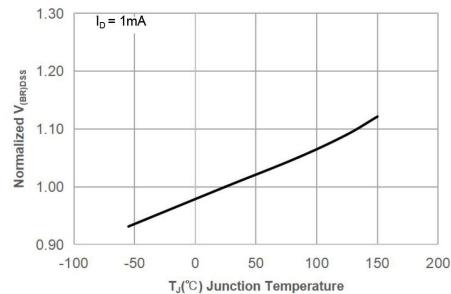


Figure 8: Normalized on Resistance vs. Junction Temperature

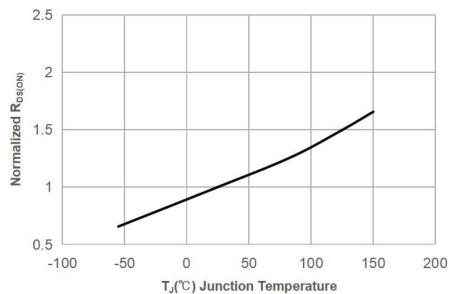


Figure 9: Maximum Safe Operating Area

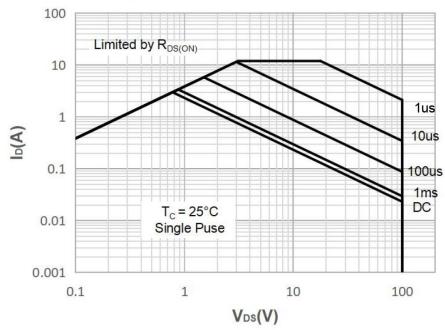


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

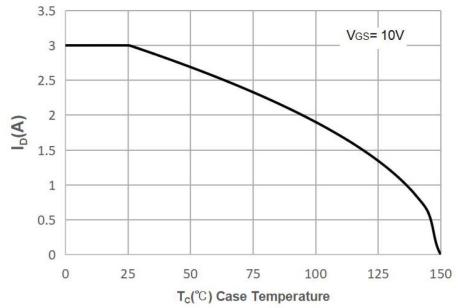


Figure 11: Normalized Maximum Transient Thermal Impedance

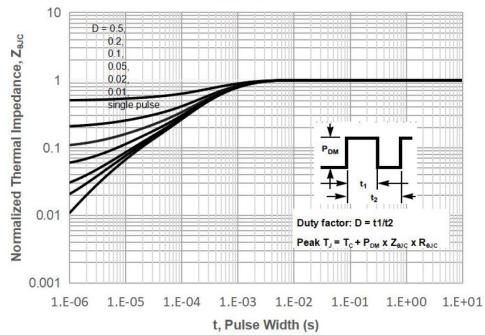
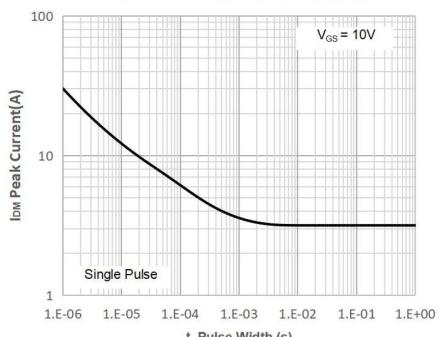


Figure 12: Peak Current Capacity



### Test Circuit

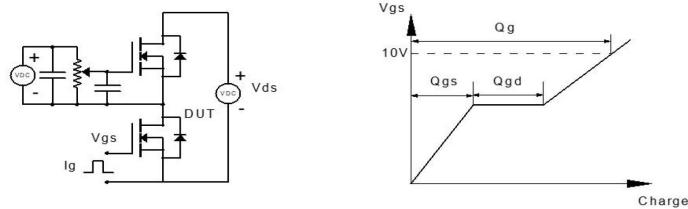


Figure 1: Gate Charge Test Circuit & Waveform

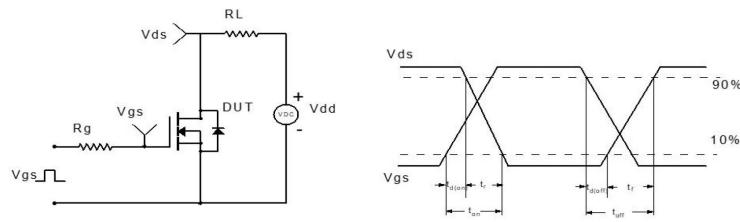


Figure 2: Resistive Switching Test Circuit & Waveform

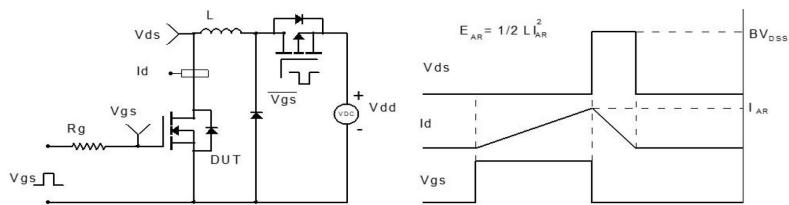


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

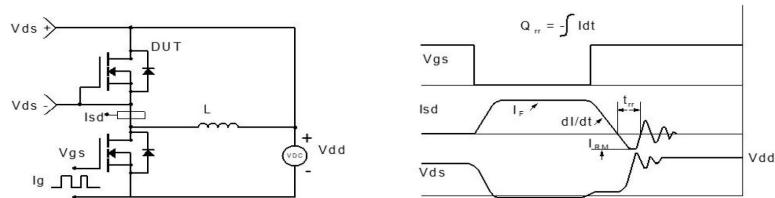
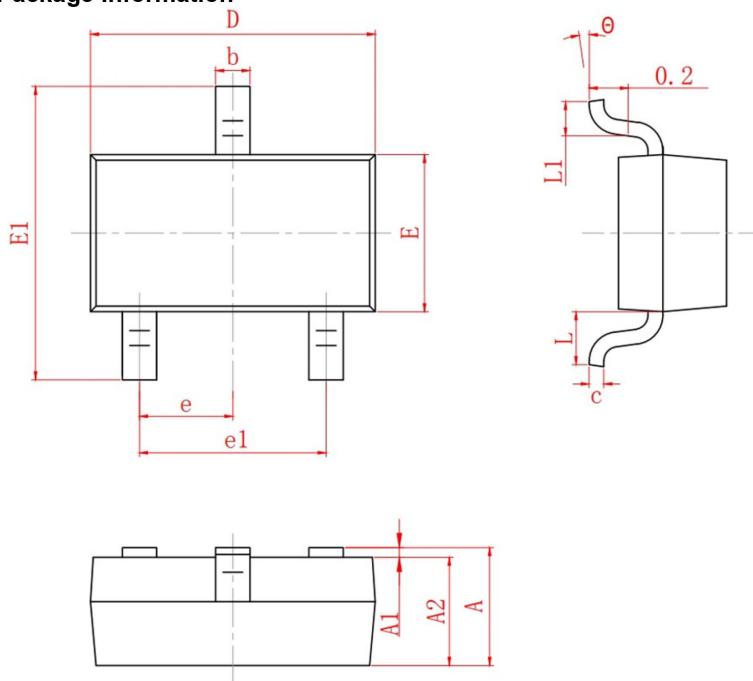


Figure 4: Diode Recovery Test Circuit & Waveform

### SOT-23 Package Information



SYMBOL	MIN	NOM	MAX
A	0.90	1.05	1.20
A1	0.00	0.05	0.10
A2	0.90	1.00	1.10
b	0.30	0.40	0.50
c	0.08	0.10	0.15
D	2.80	2.90	3.00
E	1.20	1.30	1.40
E1	2.30	2.40	2.50
L	0.30	0.40	0.50
θ	0°	5°	10°
L1	0.55 REF		
e	0.95 BSC		
e1	1.90 REF		