• General Description

The CH100P04Dcombines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

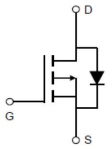
• Features

- ■ Advance high cell density Trench technology
- ■Low $R_{DS(ON)}$ to minimize conductive loss
- ■Low Gate Charge for fast switching
- ■Low Thermal resistance

•Application

- ■MB/VGA Vcore
- ■SMPS 2nd Synchronous Rectifier
- ■POL application
- ■BLDC Motor driver

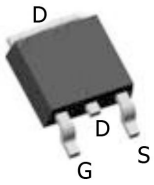
• Product Summary



V_{DS} =-40V

$R_{DS(ON)}$ < 6mΩ

I_D =-100A



TO-252

•Ordering Information:

Part NO.	CH100P04D
Marking	CH100P04D
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2500

•Absolute Maximum Ratings (T_C =25℃)

Parameter	**Symbol**	Rating	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_{D@}$TC=25℃	-100	A
	$I_{D@}$TC=75℃	-80	A
	I_{D} @TC=100℃	-70	A
Pulsed Drain Current ①	I_{DM}	-396	A
Total Power Dissipation	P_D@TC=25℃	107	W
Total Power Dissipation	P_D@TA=25℃	4.5	W
Operating Junction Temperature	T_J	-55 to 175	℃
Storage Temperature	T_{STG}	-55 to 175	℃
Single Pulse Avalanche Energy@L=0.1mH	E_{AS}	576	mJ

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	1.4	° C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	48	° C/W
Soldering temperature, wavesoldering for 10s	T_{sold}	-	-	265	° C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V,I_D =-250uA	-40			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =-250uA	-1.0	-1.7	-2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-40V, V_{GS} =0V			-1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V ,V_{DS} =0V			±100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A		4.9	6.0	mΩ
		V_{GS}=-4.5V, I_D=-20A		6.5	8.3	mΩ
Forward Transconductance	g_{FS}	V_{DS} =-5V, I_D=-20A		59		s

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	Ciss	V_{DS} =-20V V_{GS} =-0V f = 1MHz	-	6638	-	pF
Output capacitance	Coss		-	545	-	
Reverse transfer capacitance	Crss		-	345	-	

•Gate Charge characteristics(T_a = 25℃)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Qg	V_{DD} =-20V I_D =-20A V_{GS} =-10V	-	118	-	nC
Gate - Source charge	Qgs		-	13	-	
Gate - Drain charge	Qgd		-	22	-	

Note: ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

Figure 1. Output Characteristics

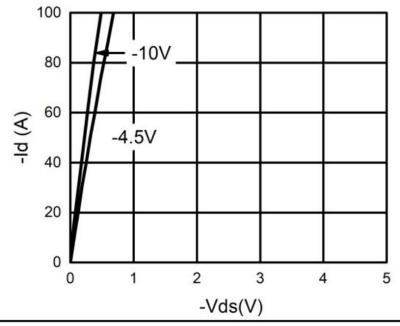


Figure 2. Transfer Characteristics

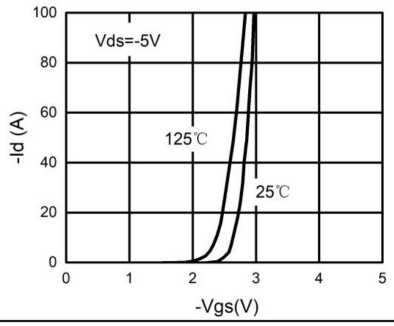


Figure 3. Power Dissipation

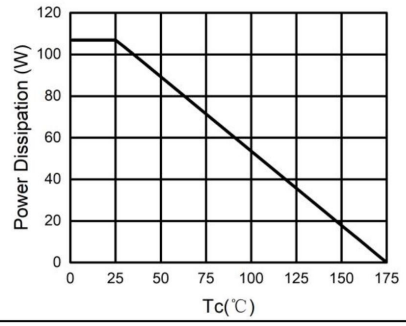


Figure 4. Drain Current

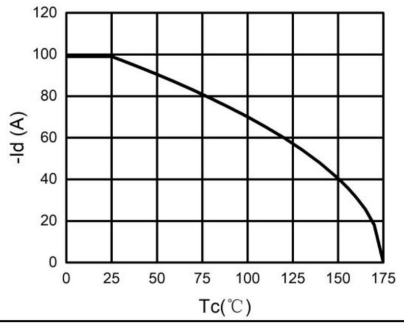


Figure 5. BV_{DSS} vs Junction Temperature

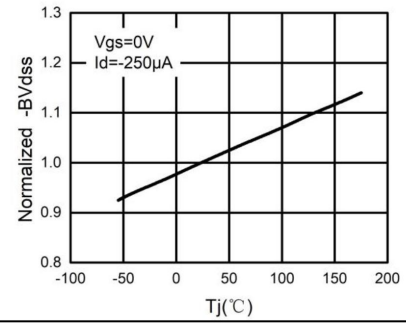


Figure 6. $R_{DS(ON)}$ vs Junction Temperature

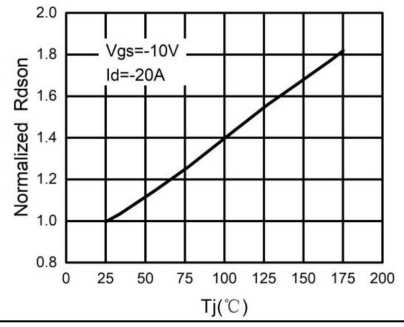


Figure 7. Gate Charge Waveforms

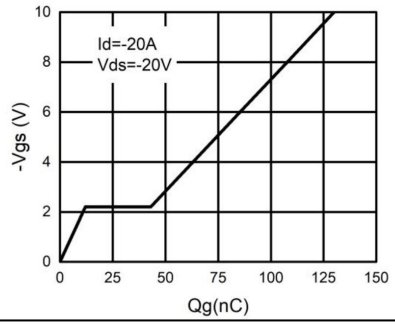


Figure 8. Capacitance

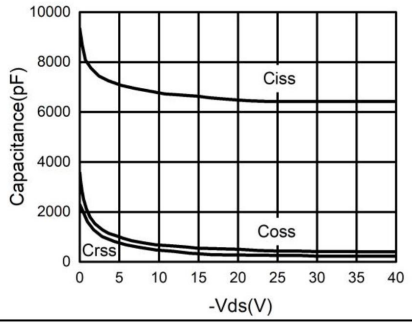


Figure 9. Body-Diode Characteristics

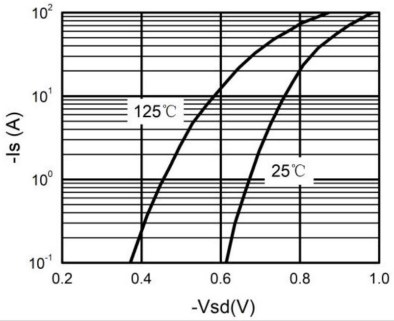
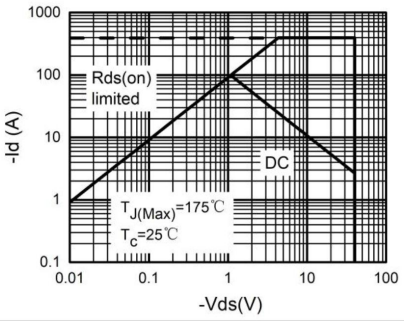
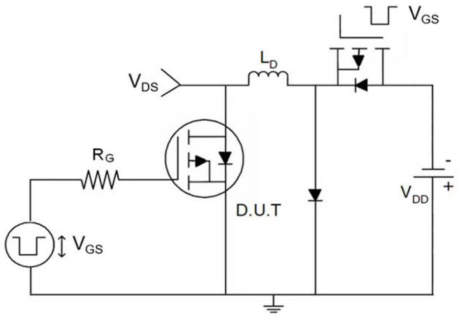


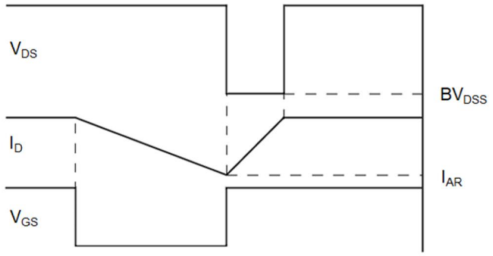
Figure 10. Maximum Safe Operating Area



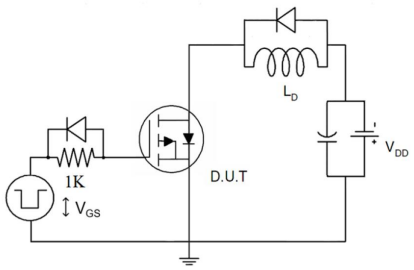
Test Circuit

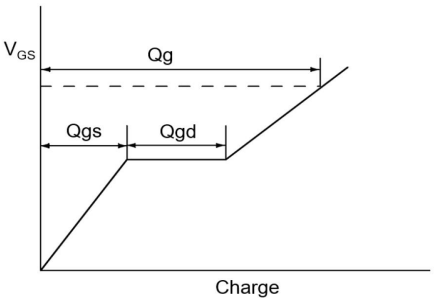
1) E_{AS} Test Circuits



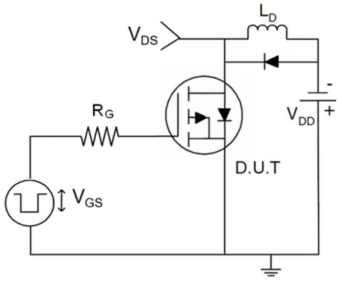


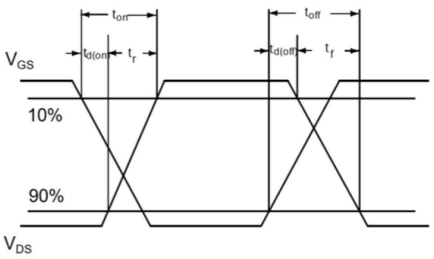
2) Gate Charge Test Circuit





3) Switch Time Test Circuit





• Dimensions (TO-252)

Unit：mm

SYMBOL	min	max	SYMBOL	min	max
A	2.10	2.50	B	0.85	1.25
b	0.50	0.80	b1	0.50	0.90
b2	0.45	0.70	C	0.45	0.70
D	6.30	6.75	D1	5.10	5.50
E	5.30	6.30	e1	2.25	2.35
L1	9.20	10.60	e2	4.45	4.75
L2	0.90	1.75	L3	0.60	1.10
K	0.00	0.23